CLAIMS

1. A phase-locked loop circuit for demodulating a Radio Data System (RDS) signal superimposed on an ARI signal component of a stereo-multiplex signal, the circuit comprising:

an oscillator that generates an in-phase component signal and a quadrature component signal of the carrier of the RDS signal;

a first circuit branch comprising a first multiplier having a first input at which a sampled stereo-multiplex signal is received and a second input at which the in-phase component signal is received, a first low-pass filter having an input connected to an output of the first multiplier, a first divider having an input connected to an output of the first low-pass filter, and a first high-pass filter having an input connected to an output of the first divider;

a second circuit branch comprising a second multiplier having a first input at which the sampled stereo-multiplex signal is received , and a second input at which the quadrature component signal is received, a second low-pass filter having an input connected to an output of the second multiplier, a second divider having an input connected to an output of the second low-pass filter, and a second high-pass filter having an input connected to an output of the second divider;

a feedback branch comprising an arithmetic unit having first and second inputs connected to outputs of the first and second high-pass filters, respectively, a clock input at which an RDS bit clock signal is received, and an output at which the arithmetic unit generates an error signal; a filter having an input at which it receives the error signal, and an output at which it generates a filtered error signal; a control unit having an input connected to the filter output, and an output connected to a control input of the oscillator at which the control unit generates a control signal in response to the error signal;

a clock generator having a first control input connected to the output of the first high-pass

filter, a second control input connected to an output of the oscillator, and an output at which the clock generator generates the RDS bit clock signal; and

an RDS decoder having a first input connected to the output of the first high-pass filter, a clock input at which the RDS bit clock signal is received, and an output from which RDS data is retrievable.

2. The phase-locked loop circuit according to Claim 1, wherein the filter comprises a loop filter.

3. The phase-locked loop circuit according to Claim 1, wherein the sampling frequency for the stereo-multiplex signal is selected such that the spectrum of the RDS signal in the region around the carrier of the RDS signal is represented completely by the sampled stereo-multiplex signal.

4. The phase-locked loop circuit according to Claim 1, wherein the sampling frequency is selected to be greater than 120 kHz.

5. The phase-locked loop circuit according to Claim 1, wherein the first and second dividers divide the low-pass filtered signals presented at their respective inputs by a division factor of 16.

6. The phase-locked loop circuit according to Claim 1, wherein the oscillator comprises a digital oscillator.

7. The phase-locked loop circuit according to Claim 1, wherein the arithmetic unit calculates the error signal at those times when the amplitude of the in-phase component is at maximum.

8. The phase-locked loop circuit according to Claim 1, wherein the oscillator is synchronized with the carrier of the RDS signal, wherein prior to synchronization, the arithmetic unit shifts the calculation cycle for the error signal by a quarter-bit clock period upon detection of a zero crossing of the amplitude of the in-phase component.

9. A method for demodulating a Radio Data System (RDS) signal superimposed on an ARI signal component of a stereo-multiplex signal, the method comprising:

generating an in-phase component signal and a quadrature component signal of the carrier of the RDS signal;

multiplying a sampled stereo-multiplex signal by the in-phase component to generate a first product signal;

low-pass filtering the first product signal to generate a first low-pass filtered signal;

dividing a sampling rate of the first low-pass-filtered signal by a first presettable division factor to generate a decimated, filtered first product signal;

high-pass filtering the decimated, filtered first product signal to generate a first high-pass-filtered signal;

decoding the first high-pass filtered signal to generate RDS data;

multiplying the sampled stereo-multiplex signal by the quadrature component of the digital oscillator to generate a second product signal;

low-pass filtering the second product signal to generate a second low-pass filtered signal;

dividing a sampling rate of the second low-pass-filtered signal by a second presettable division factor to generate a decimated, filtered second product signal;

high-pass filtering the decimated, filtered second product signal to generate a second high-

pass-filtered signal;

calculating an error signal representing a phase difference between the carrier of the RDS signal and the output signal of the oscillator based on the first and second high-pass-filtered signals and an RDS clock signal, wherein the error signal represents a phase position between the carrier of the RDS signal and the output signal of the oscillator; and

generating a correction signal for controlling the oscillator based on the error signal.

10. The method for demodulating a RDS signal according to Claim 9, further comprising the step of:

filtering the error signal prior to using the error signal to generate the correction signal.

11. The method for demodulating a RDS signal according to Claim 10, wherein the step of filtering the error signal comprises the step of:

filtering the error signal with a loop filter.

12. The method according to Claim 9, further comprising the steps of:

selecting, prior to the step of generating in-phase and quadrature component signals, a sampling frequency for the stereo-multiplex signal such that the spectrum of the RDS signal in the region around the carrier of the RDS signal is represented completely by the digital signal.

13. The method according to Claim 12, wherein the sampling frequency is selected to be greater than 120 kHz.

14. The method according to Claim 9, wherein the first presettable division factor is 16.

15. The method according to Claim 9, wherein the second presettable division factor is 16.

16. The method according to Claim 9, wherein the oscillator includes a digital oscillator.

17. The method according to Claim 9, wherein the RDS bit clock signal is generated by a clock generator in response to the oscillator and the first high-pass-filtered signal.

18. The method according to Claim 17, wherein the step of decoding the first high-pass filtered signal to generate RDS data is performed by an RDS decoder that is clocked by the RDS bit clock signal.

19. The method according to Claim 1, wherein the step of calculating the error signal is performed at those times when the amplitude of the in-phase component is at maximum.

20. The method according to Claim 1, wherein the oscillator is synchronized with the carrier of the RDS signal, and wherein the step of calculating the error signal comprises the step of:

shifting the calculation cycle for the error signal by a quarter-bit clock period upon detection of a zero crossing of the amplitude of the in-phase component.

21. The method according to Claim 1 wherein the method is implemented as a software program stored in a computer-readable medium.

22. A phase-locked loop circuit for demodulating a Radio Data System (RDS) signal superimposed on an ARI signal component of a stereo-multiplex signal, the circuit comprising:

oscillator means for generating an in-phase component signal and a quadrature component signal of an RDS carrier signal in response to an oscillator control signal;

means for generating a first product signal of a sampled stereo-multiplex signal and the in-phase component signal;

means for generating a second product signal of a sampled stereo-multiplex signal and the quadrature component signal;

means for controlling the oscillator based on the phase relationship between the RDS carrier signal and the signals generated by the oscillator; and

means for generating RDS data based on the first high-pass filter.

23. The phase-locked loop circuit according to Claim 22, wherein the means for generating a first product signal comprises:

means for multiplying a sampled stereo-multiplex signal by the in-phase component to generate a first product signal;

means for low-pass filtering the first product signal to generate a first low-pass filtered signal;

means for low-pass filtering the first product signal to generate a first low-pass filtered signal; and

means for high-pass filtering the decimated, filtered first product signal to generate a first high-pass-filtered signal.

24. The phase-locked loop circuit according to Claim 22, wherein the means for generating a second product signal comprises:

means for multiplying the sampled stereo-multiplex signal by the quadrature component of the digital oscillator to generate a second product signal;

means for low-pass filtering the second product signal to generate a second low-pass filtered signal;

means for dividing a sampling rate of the second low-pass-filtered signal by a second presettable division factor to generate a decimated, filtered second product signal; and

means for high-pass filtering the decimated, filtered second product signal to generate a second high-pass-filtered signal.

25. The phase-locked loop circuit according to Claim 22, wherein the means for controlling the oscillator comprises:

means for calculating an error signal representing a phase difference between the RDS carrier signal and the oscillator based on the first and second product signals, wherein the error signal represents a phase position between the RDS carrier signal and the output signal of the oscillator; and

means for generating the oscillator control signal based on the error signal.

26. The phase-locked loop circuit according to Claim 22, wherein the sampling frequency for the stereo-multiplex signal is selected such that the spectrum of the RDS signal in the region around the carrier of the RDS signal is represented completely by the sampled stereo-multiplex signal.

27. The phase-locked loop circuit according to Claim 22, wherein the first and second divider means divide the received low-pass filtered signals by a division factor of 16.

28. The phase-locked loop circuit according to Claim 22, wherein the arithmetic unit calculates the error signal is calculated at those times when the amplitude of the in-phase component is at maximum.

29. The phase-locked loop circuit according to Claim 25, wherein the oscillator means is synchronized with the carrier of the RDS signal, wherein prior to synchronization, wherein the means for generating an error signal shifts the calculation cycle for the error signal by a quarter-bit

4 clock period upon detection of a zero crossing of the amplitude of the in-phase component.